AMENDMENTS TO THE CLAIMS, COMPLETE LISTING OF CLAIMS IN ASCENDING ORDER WITH STATUS INDICATOR

Kindly cancel claims 8 and 11 without prejudice or disclaimer to its underlying subject matter.

7. (Currently Amended) A method of fabricating a bipolar transistor comprising the steps of:

forming on a semiconducting substrate a first insulating film having a pattern in which the surface of the semiconducting substrate is partially exposed from said first insulating film;

sequentially forming a first conductive film and a second insulating film over the surface of said semiconducting substrate formed with said first insulating film, and then forming an opening portion so as to expose the surface of said semiconducting substrate;

forming a third insulating film on said opening portion and said conductive film;

forming a first impurity diffusion layer having a first conducting type by applying ion implantation to said semiconducting substrate at a first energy through said third insulating film;

forming a second impurity diffusion layer having the first conducting type by applying ion implantation to said semiconducting substrate at a second energy;

forming a third impurity diffusion layer having the first conducting type in said semiconducting substrate connected to said first conductive layer;

forming side walls made of a fourth insulating layer on side walls of said opening portion of said semiconducting substrate in which said first, second and third impurity diffusion are formed;

forming a second conductive film in said opening portion so as to be connected to said first impurity diffusion layer; and

forming a fourth impurity diffusion layer having a second conducting type in said second impurity diffusion layer by ion implantation applied through said second conductive layer,

forming a fifth impurity diffusion layer under said first impurity diffusion layer by ion implantation at a third energy after formation of said second impurity diffusion layer by ion implantation at said second energy.

8. (Canceled).

9. (Previously Presented) A method of fabricating a bipolar transistor according to claim 7, wherein said first energy is lower than said second energy.

10. (Currently Amended) A method of fabricating a bipolar transistor comprising:

forming a graft base layer from a first impurity diffusion layer created by ion implantation, wherein said graft base layer is of a first conducting type and is formed in a semiconductor substrate;

forming a first conductive film on said semiconductor substrate which is connected to said graft base layer;

forming an opening in said first conductive film;

forming a link base layer from a second impurity diffusion layer created by ion implantation, wherein said link base layer is of the first conducting type, is formed in a portion of said semiconductor substrate which is exposed by said opening portion, and is connected to said graft base layer;

forming a base layer from a third impurity diffusion layer, wherein said base layer is of the first conducting type, is formed in said semiconductor substrate, and is formed to contain said link base layer;

forming side walls in said opening portion from an insulating film, said side walls defining a central aperture; ~~and~~

forming an emitter from a fourth impurity diffusion layer created by ion implantation, wherein said emitter is of a second conducting type, is formed in a portion of said semiconducting substrate exposed by said central aperture, is surrounded by said side walls, and is formed in said base layer; and

forming a collector from a fifth impurity diffusion layer, wherein said collector is of the second conducting type, is formed directly under said link base layer and has a maximum impurity concentration with a diffusion depth deeper than a diffusion depth for a maximum impurity concentration of said base layer;

wherein said link base layer has a diffusion depth equal to or less than a diffusion depth of said emitter layer.

11. (Canceled)

12. (Currently Amended) A method as claimed in claim ~~11~~10, further comprising reducing an impurity concentration in a lower portion of said base layer with said collector layer.

13. (Currently Amended) A method as claimed in claim ~~11~~10, further comprising forming said graft base layer with a gap therein aligned with the opening in the first conductive film.

14. (Currently Amended) A method as claimed in claim ~~11~~10, wherein said forming a link base layer further comprises forming said link bas layer on opposite sides of the emitter layer.

15. (Currently Amended) The method as claimed in claim ~~11~~10, wherein said forming a link base layer further comprises forming said link base layer with a depth of about 30 nm to 50 nm.